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Matlab Simulation of Nine Level Cascaded H-Bridge Inverter with Equal DC Voltage

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Abstract: **Multilevel inverter is used in applications that need high voltage and high current. The topologies of multilevel inverter have several advantages such as lower THD, lower EMI generation, better output waveform and higher efficiency for a given quality of output waveform. This paper presents the development of Altera FPGA as a control circuit for multilevel PWM single phase inverter. The FPGA chip produce 16 control signal for 9 level output voltage. Cyclone FPGA chip is a programmable logic device develop by Altera and can be considered as an efficient hardware for rapid prototyping. FPGA chip is chosen for the hardware implementation of control circuit is due to its high computation speed that can produce accurate control signal. Internal architecture of control circuit embeds in FPGA are described in detail. VHDL language is used to model the switching strategies and Quartus II software is used as a simulation and compiler tool. These inverter topologies with filters would have reduced harmonics and can operate at high efficiency.**

Keywords: **Field Programmable gate array (FPGA), VHDL Hardware description language, multilevel inverter, Cascaded multilevel inverter, Digital controller.**

I. INTRODUCTION

The Multilevel inverter has gained much attention in recent years due to its advantages in high power possibility with low switching frequency and low harmonics. The essential advantage of multilevel inverters is the improvement in the output voltage signal quality using devices of low voltage rating with lesser switching frequency, thereby increasing the overall efficiency of the system. The general function of the multilevel inverter is to synthesize a desired high voltage from several levels of dc voltages. The dc sources can be batteries, fuel cells, etc., where all the dc levels are considered to be identical. The performance of the multilevel inverter is better than a classical inverter. The total harmonic distortion of the classical inverter is very high. In other words the total harmonic distortion for multilevel inverter is low. The diode clamped inverter provides multiple voltage levels from a series bank of capacitors. The voltage across the switches is only half of the DC bus voltage. These features effectively double the power rating of voltage source inverter for a given semiconductor device.

A Field-programmable Gate Array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping, partial re-configuration of the portion of the design and the low non-recurring engineering costs relative to an ASIC design (notwithstanding the generally higher unit cost), offer advantages for many applications. Vendors can also take a middle road by developing their hardware on ordinary FPGAs, but manufacture their final version so it can no longer be modified after the design has been committed. Some FPGAs have the capability of partial re-configuration that lets one portion of the device be re-programmed while other portions continue running.

In the last few years. Field Programmable Gate Array circuits (FPGA) are becoming popular in those applications where high performance, low development and production cost and fast time-to market are major issues [1]-[4]. In fact, they are

functionally similar to standard ASICs but appear cost effective even in small-medium volume productions, thus allowing, also in these cases, the realization of powerful and cheap systems. Additionally, they almost eliminate the code portability problem as VHDL, the main hardware description language, and several development tools are almost device independent. One field which can obtain significant advantages by the use of FPGA is multilevel converters [2]. This is because the high number of switching components require a high number of output signals, needed to apply the modulation pattem to power devices and most microcontrollers are not able to satisfy this demand. In fact, they can only generate few of them (generally six). because they are designed to control standard inverters. Multilevel converters, moreover, often require complex control algorithms which cannot be implemented in real-time using standard low cost microcontrollers or DSP, but can be successful implemented using hardware description languages and FPGA.

II. THE OPERATION OF MODULAR H-BRIDGE

MSMI (Modular Structured Multilevel Inverter) circuit is shown in Figure 1. MSMI consists of (n-1)/2 number of single phase H-Bridge inverters that are connected in series to generate n level of output phase voltage. A single-phase structure of a single-phase MSMI with 9 level of output is shown in Figure 1. The output phase voltage is equal to the summation of each H-Bridge module given by the following formula.

V0 = Vm1 + Vm2 + ……+ Vmh

Where h is the number of H-Bridge modules used in the multilevel circuit.

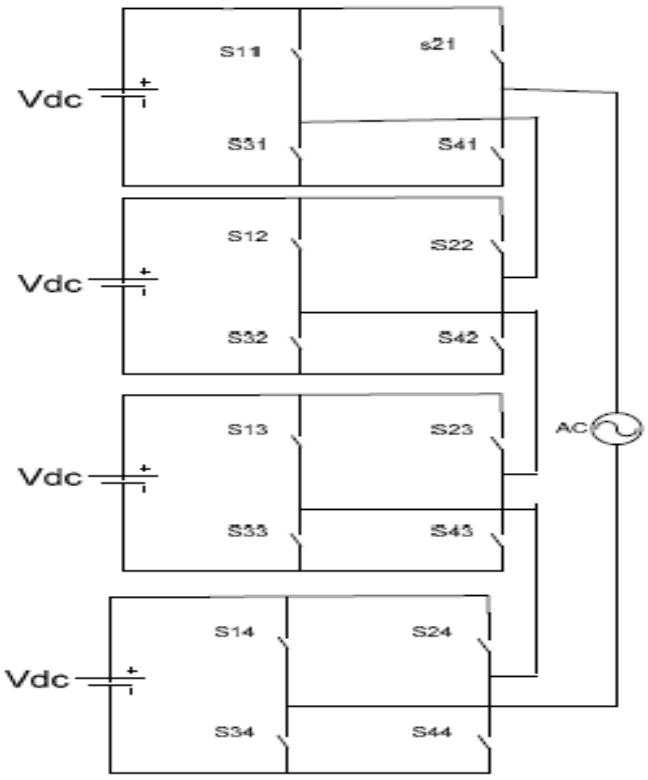

Fig.1- MSMI connection for 9 level of output phase voltage

The circuit diagram shows a 4 bridge H-bridge. This is symmetrical. That is, all the voltages of each bridge is the same (V1=V2=V3=V4).The bridges are connected in series. We have designed this circuit for 9-level multilevel inverter.

Number of bridges is found by, No.of bridges= (n-1)/2

Where, n is the level of the inverter.

Here the level to be obtained is 9 and hence the number of bridge is 4.

Each bridge consists of 4 switches each.

Switch can be IGBT, MOSFET or any other power electronic devices.

Each bridge provides 3 numbers of levels. For one bridge(-1,0,1),so for four bridge(-4,-3,-2,-1,0,1,2,3,4).

A. Block Diagram Of The System:

FPGA CHIP:

The most common FPGA consists of an array of logic blocks (called Configurable Logic Block, CLB, or Logic Array Block, LAB, depending on vendor), I/O pads, and routing channels. Generally, all the routing channels have the same width (number of wires). Multiple I/O pads may fit into the height of one row or the width of one column in the array.

OPTOISOLATOR:

The main purpose of an opto-isolator is "to prevent high voltages or rapidly changing voltages on one side of the circuit from damaging components or distorting transmissions on the other side". Commercially available opto-isolators withstand input-to-output voltages up to 10 kV and voltage transients with speeds up to 10 kV/μs. Here the optoisolator is for providing grounding between the FPGA chip and the inverter.

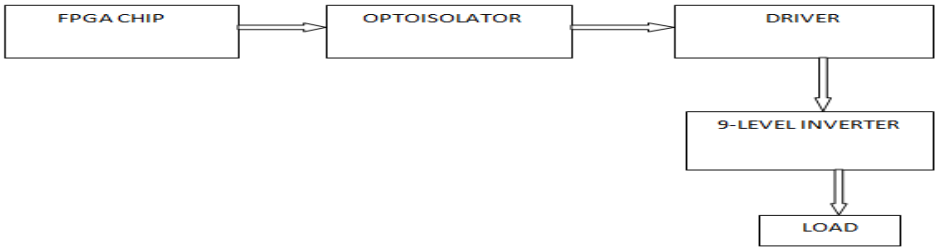

Fig. 2- Block diagram of overall system

DRIVER:

This is used for the proper operation of the switches. This makes the switch ON or OFF.

9-LEVEL INVERTER:

An inverter is an electrical device that converts direct current (DC) to alternating current (AC); the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits.

LOAD:

From a load point of view, this spectrum analysis is more attractive in active filtering applications. It is also interesting for the understanding of the behaviour of a given system in variable speed drive applications, if the power converter is fed through separated dc-voltage sources (dc-dc resonant converters, photo-voltaic cells, fuel cells …)

B. Internal Architecture of Control Unit Embedded In Fpga Chip:

The internal structure of the proposed multilevel control circuit using MSMI technique is shown in Figure 3. VHDL code is used to model all of the module and Quartus II software is used as the design tools. The input clock with frequency 48MHz is divided by 100KHz and 1 Mhz by clock divider module. The structure consists of a storage unit to store the pre-calculated switching signal.

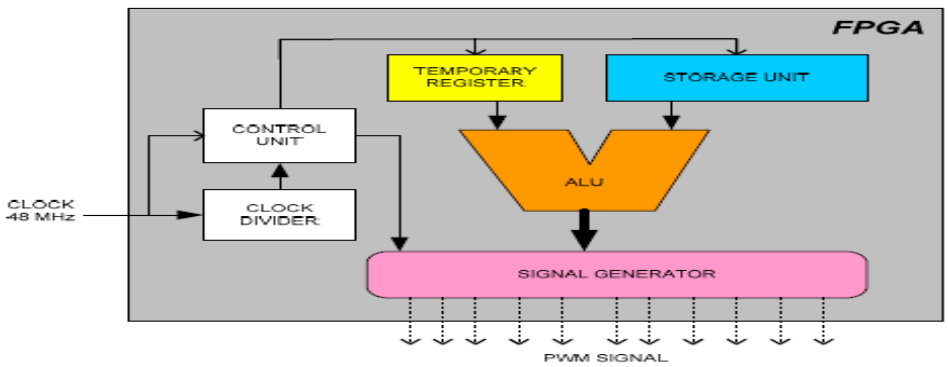

Fig. 3- Architecture of control circuit embeds in FPGA

Temporary register is used to latch data from control unit, which are then compared with the pre-calculated data in storage unit. The comparison process is done in arithmetic logic unit (ALU). The output from ALU is transferred to signal generator module. This module will produce 16 channel output signal that is used to control opt isolator circuit.

III. SIMULATION AND EXPERIMENTAL RESULTS

The 16 channel control signal for 9 level output phase voltage are shown in Figure 4. The switching time is 1KHz. The output result from the multilevel circuit is shown in Figure 5.

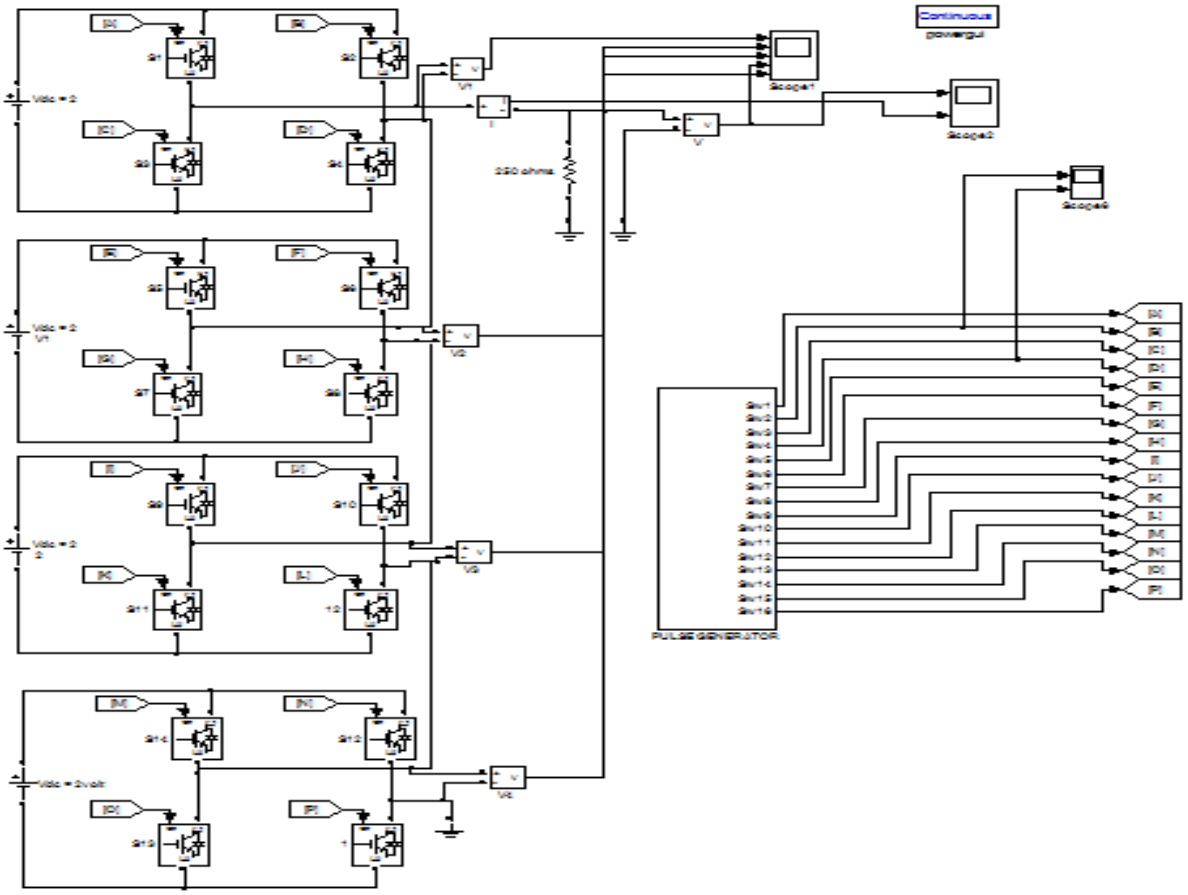

Fig. 4- Simulation Circuit with R load

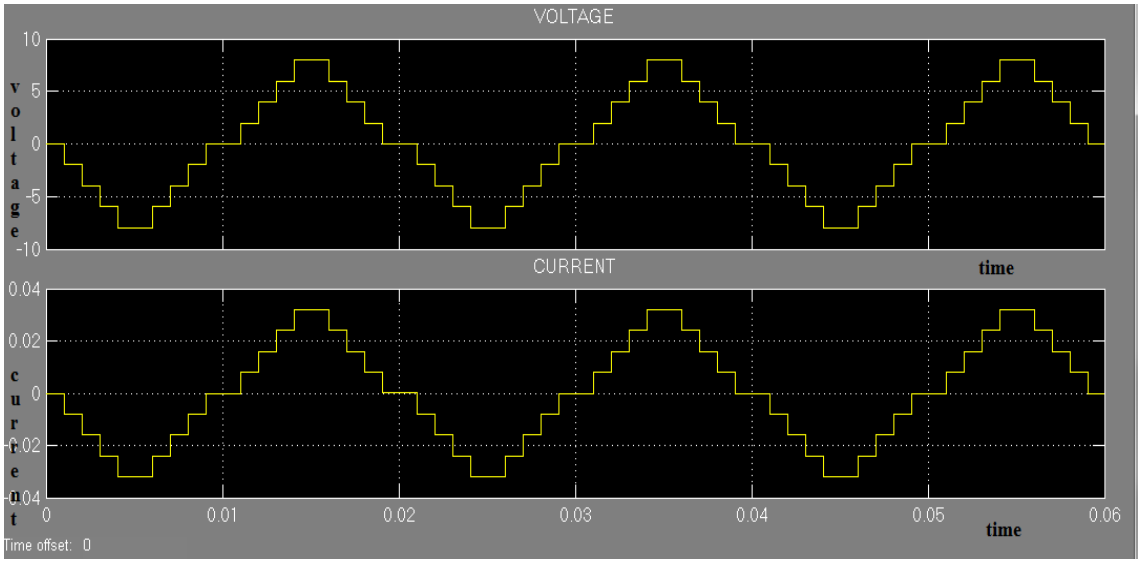

Fig. 5- Simulation results with R load

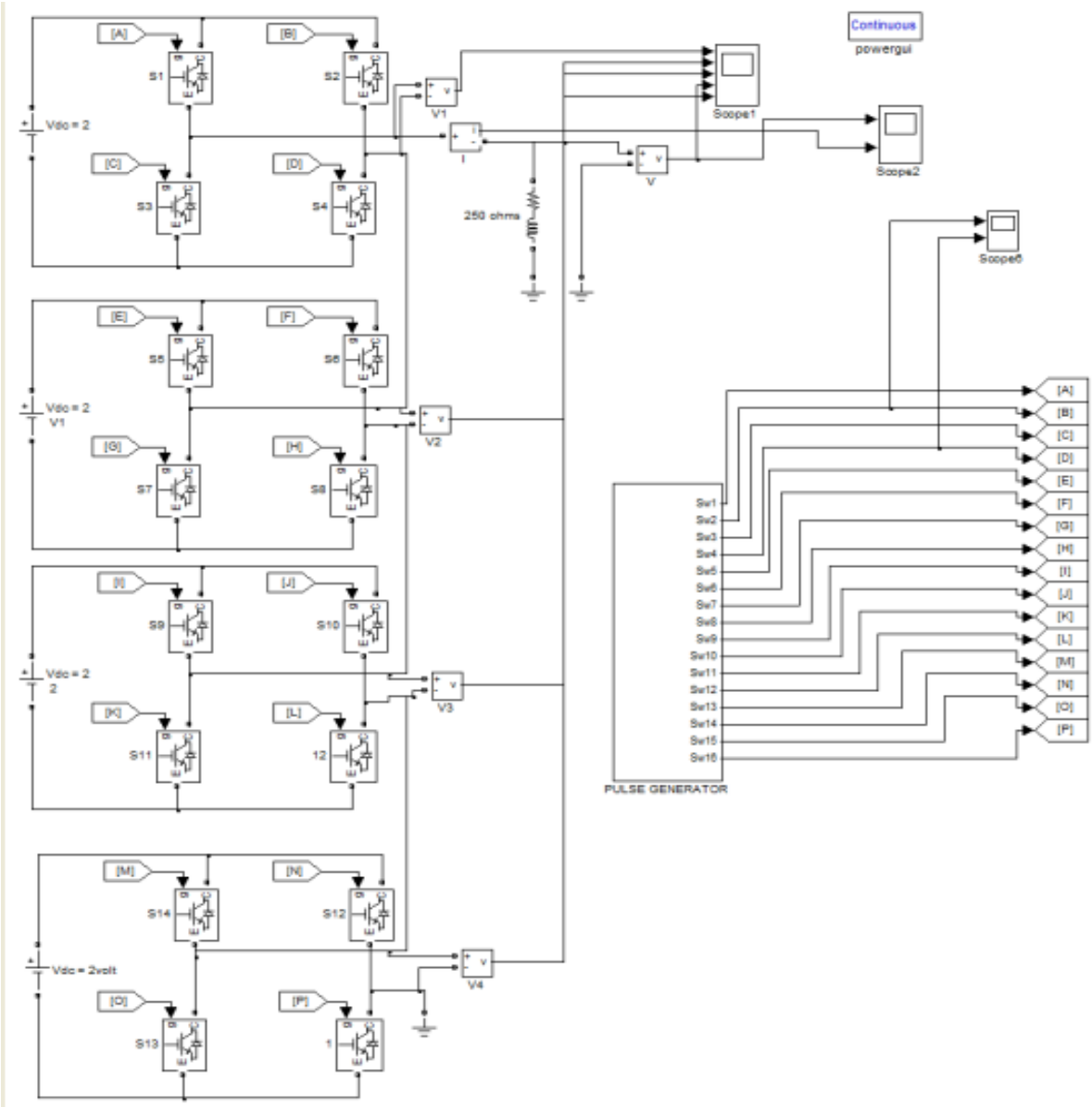

Fig. 6- Simulation Circuit with RL load

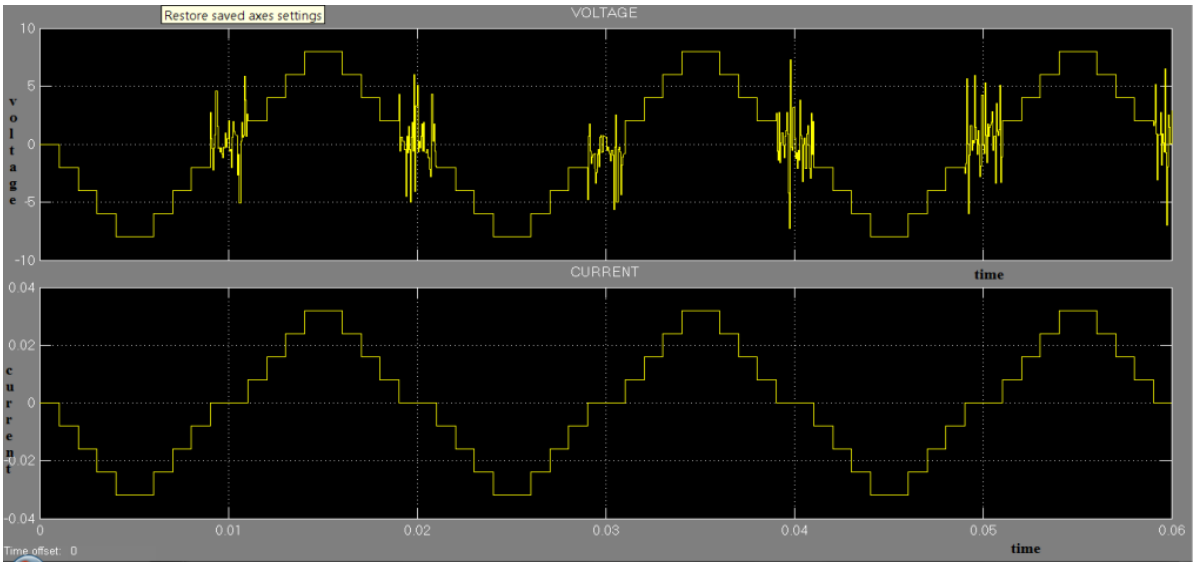

Fig. 7- Simulation result with RL load

IV. CONCLUSION

FPGA based control circuit for multilevel inverter was successfully realized. This was accomplished by using Altera Cyclone FPGA chip to compute and generate PWM signals with 1 KHz switching frequency to produce nine level multilevel output voltages. The design is simulated and compiled using Quartus II software and the compilations results consists of 1250 logic elements. In this project the development of Altera FPGA as a control circuit for multilevel PWM single phase inverter was successfully implemented. The simulation output for multilevel inverter was obtained with MATLAB. The FPGA chip produce 16 control signal for 9 level output voltage. Recently, progress of PLD (Programmable Logic Device) like FPGA or CPLD makes it realize the digital control system of power electronics without microprocessor (CPU or DSP).

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